CLAIMS

1. A pre-correlation filter for a receiver that receives spread-spectrum signals, the filter including:

an array of complex accumulation registers that over multiple code chips accumulate measurements that correspond to samples of the received signal, the accumulation registers being associated with code chip ranges that span all or a portion of a code chip;

a code phase decoder that controls the respective complex accumulation registers to direct respective measurements to the complex accumulation registers that are associated with the code chip ranges from which the samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the sample.

2. The pre-correlation filter of claim 1, wherein the code chip ranges covering a rising edge of the code chip are smaller than the code chip ranges covering other sections of the code chip.

3. The pre-correlation filter of claim 1, wherein the code chip ranges are adjustable.

4. The pre-correlation filter of claim 1 wherein the sizes, numbers and starting points of the code chip ranges are selectively varied.

5. The pre-correlation filter of claim 4 wherein the code chip ranges that include an estimated location of the chip edges in a direct path signal are narrowed.

6. The pre-correlation filter of claim 4 wherein the starting points of one or more code chip ranges are changed to selectively position the code chip ranges relative to the estimated location of chip edges in a direct path signal.

7. The pre-correlation filter of claim 4 wherein the number of code chip ranges is reduced after an estimate of the location of chip edges in a direct path signal is calculated.

8. The pre-correlation filter of claim 1, wherein the respective complex accumulation registers include inphase registers that collect measurements that correspond to inphase samples and quadrature phase registers that collect measurements that correspond to quadrature samples.

9. The pre-correlation filter of claim 1 wherein the array of complex accumulation values are compared with a predetermined reference shape to detect the presence or absence of interfering signals.

10. A receiver for receiving spread-spectrum signals, the receiver including:

a local code generator that produces phase-delayed versions of a code that is included in the received signal;

a plurality of multipliers that multiply the respective versions of the code by samples taken of the received signal and produce corresponding measurements;

a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase;

a carrier phase generator that produces phase angles that correspond to an estimated carrier phase;

a code tracking delay lock loop that produces code error signals that are used to control the code rate of the code generator;

a carrier tracking phase lock loop that produces phase error signals that are used to control the phase generator;

a pre-correlation filter that includes

an array of complex accumulation registers that collect measurements that correspond to samples of the received signal, the accumulation registers being associated with code chip ranges that span all or a portion of a code chip;

a code phase decoder that controls the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are associated with the code chip ranges from which the associated samples are taken, the

code phase decoder decoding values that correspond to the estimated phase angles of the samples;

a multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce code multipath error signals and carrier multipath error signals; and

adders that combine the code multipath error signals and carrier multipath error signals with the code error signals and phase errors signals, respectively, to correct for code and carrier tracking errors associated with multipath interference, the adders producing the signals that are used to control the code generator and the phase generator.

11. The receiver of claim 10, wherein the code chip ranges covering a rising edge of the code chip are smaller than the code chip ranges covering other sections of the code chip.

12. The receiver of claim 10, wherein the code chip ranges are adjustable.

13. The pre-correlation filter of claim 10 wherein the sizes, numbers and starting points of the code chip ranges are selectively varied.

14. The pre-correlation filter of claim 10 wherein the code chip ranges that include an estimated location of the chip edges in a direct path signal are narrowed.

15. The pre-correlation filter of claim 10 wherein the starting points of one or more code chip ranges are changed to selectively position the code chip ranges relative to the estimated location of the chip edges in a direct path signal.

16. The pre-correlation filter of claim 10 wherein the number of code chip ranges is reduced after an estimate of the location of chip edges in a direct path signal is calculated.

17. The receiver claim 10, wherein the respective complex accumulation registers include inphase registers that collect measurements that correspond to inphase samples and quadrature registers that collect measurements that correspond to quadrature samples.

18. The receiver of claim 10, wherein the multipath mitigation processor combines the measurements collected by groups of complex accumulators to produce multiple early and late correlation values.

19. The receiver of claim 10 wherein the array of complex accumulation values are compared with a predetermined reference shape to detect the presence or absence of interfering signals.

20. The receiver of claim 10 wherein the multipath mitigation processor further produces code offset and carrier phase values that are used in place of the code error and phase error signals to control the carrier phase generator and the code phase generator.

21. A receiver for receiving spread-spectrum signals, the receiver including:

a local code generator that produces a phase-delayed version of a code that is included in the received signal;

a code phase generator that produces chip edge signals and code phase angles that correspond to an estimated code phase;

a multiplier that multiplies the version of the code by samples taken of the received signal and produces corresponding measurements;

a carrier phase generator that produces phase angles that correspond to an estimated carrier phase;

a pre-correlation filter that includes

an array of complex accumulation registers that collect measurements that correspond to samples of the received signal, the accumulation registers being associated with code chip ranges that span all or a portion of a code chip;

a code phase decoder that controls the complex accumulation registers to direct the measurements to the respective complex accumulation registers that are

associated with the code chip ranges from which the associated samples are taken, the code phase decoder decoding values that correspond to the estimated phase angles of the samples;

a multipath mitigation processor that uses the measurements collected by the complex accumulation registers to produce direct path code offset and phase angle signals that are used to control the code generator and the phase generator.

22. The receiver of claim 21, wherein the multipath mitigation processor combines the measurements collected by groups of complex accumulators to produce early and late correlation values.

23. The receiver of claim 21, wherein the multipath mitigation processor combines the measurements collected by groups of complex accumulators to produce multiple early and late correlation values.

24. The receiver of claim 21, wherein the code chip ranges covering a rising edge of the code chip are smaller than the code chip ranges covering other sections of the code chip.

25. The receiver of claim 21, wherein the code chip ranges are adjustable.

26. The pre-correlation filter of claim 21 wherein the sizes, numbers and starting points of the code chip ranges are selectively varied.

27. The pre-correlation filter of claim 21 wherein the code chip ranges that include an estimated location of the chip edges in a direct path signal are narrowed.

28. The pre-correlation filter of claim 21 wherein the starting points of one or more code chip ranges are changed to selectively position the code chip ranges relative to the estimated location of the chip edges in a direct path signal.

29. The pre-correlation filter of claim 21 wherein the number of code chip ranges is reduced after an estimate of the location of chip edges in a direct path signal is calculated.

30. The receiver claim 21, wherein the respective complex accumulation registers include inphase registers that collect measurements that correspond to inphase samples and quadrature registers that collect measurements that correspond to quadrature samples.

31. The receiver of claim 21 wherein the array of complex accumulation values are compared with a predetermined reference shape to detect the presence or absence of interfering signals.